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Transmitted herewith for filing is the patent application of:

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Tetsurou TOUBOU
FOR: SIGNAL TRANSMISSION CIRCUIT

Enclosed are:

- 56 pages of specification, claims, abstract.
 Declaration and Power of Attorney.
 Priority Claimed.
 Certified copy of Japanese Patent Application No. 11-325062
 11 sheets of formal drawing.
 An assignment of the invention to Matsushita Electric Industrial Co., Ltd.
 and the assignment recordation fee.
 An associate power of attorney.
 A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27.
 Information Disclosure Statement, Form PTO-1449 and reference.
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The filing fee has been calculated as shown below:

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Total Claims	19	-20	\$18.00	\$0.00
Independent Claims	15	-3	\$80.00	\$1,040.00
Multiple Dependent Claim(s)				\$0.00
Basic Fee				\$710.00
Total of Above Calculations				\$1,750.00
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Assignment & Recording Fee				\$40.00
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Respectfully submitted,

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SIGNAL TRANSMISSION CIRCUIT

BACKGROUND OF THE INVENTION

The present invention relates to a design technique for 5 digital circuits. In particular, the present invention relates to a technique for speeding up signal transmission and a technique for reducing power consumption of the circuits.

In the current multimedia era, there is a demand for 10 higher speed operational performance in fixed equipment, and lower power consumption in portable equipment. With these trends, a demand for high speed and low power consumption of semiconductor integrated circuits has become increasingly strong. On the other hand, under the promotion of 15 miniaturization in the semiconductor process and multilayering of wiring, parasitic devices in wiring significantly affect the design. For example, an increase of the wiring resistance value and the wiring inductance value due to a reduction of the thickness of films for metal wiring 20 and an increase of the wiring capacitance value due to a reduction of wiring pitch tend to prevent the achievement of high speed semiconductor integrated circuits and low power consumption.

Japanese Laid-Open Patent Publication No. 2-285711 25 discloses a signal transmission circuit for transmitting digital signals. In this signal transmission circuit, in order to realize high-speed driving of the signal line having

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5 a large load capacity, the voltage of a signal line is set to
an intermediate voltage between a logic high voltage (Vdd)
and a logic low voltage (Vss), and the signal line is driven
to the logic high voltage or the logic low voltage by an
inverter.

6
7 In this conventional signal transmission circuit, the
8 voltage magnitude of the signal line (assuming Vss = 0, the
9 voltage magnitude is Vdd/2) is large. Therefore, it takes a
long time to set the voltage of the signal line to an
10 intermediate voltage, and the power consumption becomes large.

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synchronization with a clock signal that repeats a first logic level indicating a preparation period and a second logic level indicating a transmission period. The first circuit block includes a transmitting circuit including a 5 transmitting capacitor, an input switch setting a voltage in accordance with a logic level of a supplied input digital signal in the transmitting capacitor at each preparation period, and a transmitting switch for generating a small voltage change in the signal line at each transmission period, 10 the voltage change being in accordance with the voltage of the transmitting capacitor that is set during the preceding preparation period. The second circuit block includes a receiving circuit including an inverter connected to the signal line, a receiving capacitor inserted between an input 15 terminal and an output terminal of the inverter, an equalizing switch for short-circuiting the input terminal and the output terminal of the inverter so as to set the voltage of the signal line to a predetermined voltage at each preparation period, and a latch for supplying an output 20 digital signal obtained by performing logic amplification of the voltage of the output terminal of the inverter for each transmission period and holding the output digital signal obtained during the preceding transmission period for each preparation period.

25 Furthermore, a second signal transmission circuit of the present invention is an asynchronous signal transmission circuit for transmitting a digital signal from a first

circuit block to a second circuit block via a signal line. The first circuit block includes a transmitting circuit including a transition detection circuit for sequentially detecting a transition of the logic level of a supplied input digital signal so as to detect a high level period during which a logic high level is output to the signal line, and a low level period during which a logic low level is output to the signal line, first and second transmitting capacitors, a precharge switch for setting a predetermined logic high voltage in the first transmitting capacitor at each low level period, a first transmitting switch for generating a small voltage change in the signal line at each high level period, the voltage change being in accordance with the voltage of the first transmitting capacitor that is set during the preceding low level period, a predischarge switch for setting a predetermined logic low voltage in the second transmitting capacitor at each high level period, and a second transmitting switch for generating a small voltage change in the signal line at each low level period, the voltage change being in accordance with the voltage of the second transmitting capacitor that is set during the preceding high level period. The second circuit block includes a receiving circuit including an inverter for amplifying a small voltage change in the signal line, a receiving capacitor inserted between an input terminal and an output terminal of the inverter, an equalizing switch inserted between the input terminal and the output terminal of the inverter, a first

level circuit for supplying a first detection signal when a small positive voltage change in the signal line is detected from the voltage of the output terminal of the inverter, a second level circuit for supplying a second detection signal 5 when a small negative voltage change in the signal line is detected from the voltage of the output terminal of the inverter, an output circuit for supplying an output digital signal having a logic level in accordance with a logic level of the input digital signal, in accordance with the first and 10 second detection signals, and an equalizing control circuit for forcing the equalizing switch to be on for a certain period after the first detection signal or the second detection signal is supplied so as to set the voltage of the signal line to a predetermined voltage.

15 This and other advantages of the present invention will become apparent to those skilled in the art upon reading and understanding the following detailed description with reference to the accompanying figures.

20 **BRIEF DESCRIPTION OF THE DRAWINGS**

Figure 1 is a circuit diagram illustrating an example of the configuration of a synchronous signal transmission circuit of the present invention.

25 Figure 2 is a circuit diagram illustrating a variation of the receiving circuit in Figure 1.

Figure 3 is a circuit diagram illustrating another variation of the receiving circuit in Figure 1.

Figure 4 is a block diagram illustrating another example of the configuration of a synchronous signal transmission circuit of the present invention.

Figure 5 is a circuit diagram illustrating the internal configuration of the transmitting circuit in Figure 4.

Figure 6 is a circuit diagram illustrating the internal configuration of the receiving circuit in Figure 4.

Figure 7 is a block diagram illustrating still another example of the configuration of a synchronous signal transmission circuit of the present invention.

Figure 8 is a block diagram illustrating an example of the configuration of an asynchronous signal transmission circuit of the present invention.

Figure 9 is a circuit diagram illustrating the internal configuration of the transmitting circuit in Figure 8.

Figure 10 is a circuit diagram illustrating the internal configuration of the receiving circuit in Figure 8.

Figure 11 is a block diagram illustrating another example of the configuration of an asynchronous signal transmission circuit of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Hereinafter, the embodiments of the present invention will be described with reference to the accompanying drawings.

Figure 1 shows an example of the configuration of a synchronous signal transmission circuit of the present invention. The signal transmission circuit in Figure 1 is a

circuit for transmitting digital signals from a first circuit block **BK1** to a second circuit block **BK2** via a signal line 30 in synchronization with a clock (CLK) signal. The circuit blocks **BK1** and **BK2** may be in the same semiconductor 5 integrated circuit or in different semiconductor integrated circuits. The signal line 30 is shown in Figure 1 by an equivalent circuit of a combination of a wiring resistance R and a wiring capacitance C . In the description below, the logic high level (H level) and the logic low level (L level) 10 of a CLK signal represent a preparation period and a transmission period, respectively. Herein, the preparation period refers to a period for preparing signal transmission, and the transmission period refers to a period for performing signal transmission.

15 The first circuit block **BK1** includes a transmitting circuit 100 having an input terminal **TIN** for receiving a digital signal to be transmitted from the internal portion of the circuit block **BK1** and an output terminal **TOUT** connected to the signal line 30. The transmitting circuit 100 includes 20 a transmitting capacitor 101, an input switch 102, a transmitting switch 103 and an inverter 104. The input switch 102 is turned on so as to supply an input digital signal to the transmitting capacitor 101 for each preparation period (a period of CLK = H) and is turned off for each 25 transmission period (a period of CLK = L). In other words, at each preparation period, the voltage in accordance with the logic level of a supplied digital signal is set in the

transmitting capacitor 101. The transmitting switch 103 is turned on so as to connect the transmitting capacitor 101 to the signal line 30 for each transmission period (a period of CLK = L) and is turned off for each preparation period (a period of CLK = H). In other words, at each transmission period, a small voltage change in accordance with the voltage of the transmitting capacitor 101 set during the preceding preparation period occurs in the signal line 30.

The second circuit block BK2 includes a receiving circuit 200 having an input terminal RIN connected to the signal line 30 and an output terminal ROUT for supplying a received digital signal to the internal portion of the circuit block BK2. The receiving circuit 200 includes an amplifier circuit 300 including a CMOS inverter 305, and a latch 310. Reference numeral 201 denotes a receiving capacitor and reference numeral 204 denotes an equalizing switch. The inverter 305 includes a p-channel MOS transistor 202 and an n-channel MOS transistor 203 that are inserted between a Vdd power line and a Vss power line, and the input terminal thereof is connected to the signal line 30. The receiving capacitor 201 and the equalizing switch 204 are inserted between the input terminal and the output terminal of the inverter 305. The equalizing switch 204 is turned on so as to short-circuit the input terminal and the output terminal of the inverter 305 for each preparation period (a period of CLK = H), and is turned off for each transmission period (a period of CLK = L) so as to allow the operation of

the inverter 305 for amplifying a small voltage change in the signal line 30 to charge and discharge the receiving capacitor 201. The equalizing switch 204 is turned on for each preparation period, so that each voltage of the signal line 30 and the input terminal and the output terminal of the inverter 305 is set to a predetermined equalized voltage V_{eq} at each preparation period. Herein, V_{eq} is a voltage determined by the input/output characteristics of the inverter 305. The latch 310 includes, for example two switches 205 and 208 and three inverters 206, 207 and 209, so as to supply an output digital signal obtained by performing logic amplification of the voltage of the output terminal of the inverter 305 for each transmission period (a period of $CLK = L$) and hold the output digital signal obtained during the preceding transmission period for each preparation period (a period of $CLK = H$). The receiving capacitor 201 may be realized by a parasitic capacitance between the gate and the drain of each of the transistors 202 and 203 constituting the CMOS inverter 305.

According to the signal transmission circuit in Figure 1, the equalizing switch 204 in the receiving circuit 200 functions to set the voltage of the signal line 30 to an equalized voltage V_{eq} . When focusing on a given preparation period, in this period, charges in an amount corresponding to the logic level of the input digital signal supplied to the transmitting circuit 100 are accumulated in the transmitting capacitor 101. The voltage of the signal line 30 in the next

transmission period changes by $+\Delta V$ or $-\Delta V$ from the equalized voltage V_{eq} depending on the amount of the charge accumulated in the transmitting capacitor 101 during the previous preparation period. Herein, ΔV is a voltage magnitude smaller than the voltage magnitude ($V_{dd}/2$) of the signal line of the conventional example. In other words, the configuration of Figure 1 can realize high-speed transmission and low power consumption because the input digital signal is converted to a signal with a small amplitude on the signal line 30.

When the voltage gain of the inverter 305 is represented by G ($= -5$ to -1000), the input capacitance value of the receiving circuit 200 on the side of the input terminal R_{IN} is $(1-G)$ times the actual capacitance value of the receiving capacitor 201. Therefore, the input capacitance value of the receiving circuit 200 can be significantly larger than the capacitance value of the transmitting capacitor 101 or the total value of the wiring capacitance C . Therefore, almost all the charges supplied from the transmitting capacitor 101 to the signal line 30 during each transmission period transfers to the receiving capacitor 201.

The capacitance value of the transmitting capacitor 101 is set to a small value. The time constant of the charge and the discharge of the transmitting circuit 100 during the transmission period is significantly small, because the time constant is determined by the product of the capacitance

value of the transmitting capacitor 101 and the on-resistance value of the transmitting switch 103. Therefore, charges rapidly transfer from the transmitting capacitor 101 to the receiving capacitor 201. Moreover, since the energy of the 5 transmission signal is small, reflection of the signal hardly occurs, even if an inductance component is contained in the signal line 30. In addition, since the capacitance value of the transmitting capacitor 101 is small, there is little influence of the power supply inductance and the wiring 10 inductance.

The transmitting circuit 100 and the receiving circuit 200 in Figure 1 can be regarded as constituting a master slave flip flop. In other words, a long wire (signal line 30) is disposed between a master latch (transmitting circuit 100) and a slave latch (receiving circuit 200). Thus, in 15 this case, power consumption can be reduced, compared with the case where the long wire is driven by an inverter. It is possible to connect a plurality of receiving circuits 200 to the signal line 30.

20 Figure 2 shows a variation of the receiving circuit 200 in Figure 1. The receiving circuit 200a in Figure 2 includes a cut-off switch 210 for separating the CMOS inverter 305 from the Vss power line after the CMOS inverter 305 completes setting the equalized voltage V_{eq} at each preparation period 25 (a period of $CLK = H$). An inverter 211 in Figure 2 constitutes a delay circuit for delaying the CLK signal.

When the equalizing switch 204 is turned on at each

preparation period, the input terminal and the output terminal of the CMOS inverter 305 are short-circuited. As a result, the voltages of the input terminal and the output terminal are set to a predetermined equalized voltage V_{eq} 5 (assuming $V_{ss} = 0$, $V_{eq} = V_{dd}/2$ for example). In this state, since both the p-channel MOS transistor 202 and the n-channel MOS transistor 203 which constitute the CMOS inverter 305 have been turned on, a through-current flows from the V_{dd} power line to the V_{ss} power line through the CMOS inverter 10 305. This through-current is unnecessary after the equalized voltage V_{eq} is completed to be set. Therefore, after a predetermined period of time has passed since the rise transition time of a CLK signal, the cut-off switch 210 cuts off the through-current of the CMOS inverter 305. Thus, 15 power consumption of the receiving circuit 200a is reduced.

Figure 3 shows another variation of the receiving circuit 200 in Figure 1. The receiving circuit 200b in Figure 3 includes a first cut-off switch 212 for separating the CMOS inverter 305 from the V_{ss} power line after the CMOS 20 inverter 305 completes setting the equalized voltage V_{eq} at each preparation period (a period of $CLK = H$) and a second cut-off switch 213 for separating the CMOS inverter 305 from the V_{ss} power line after the voltage of the output terminal of the CMOS inverter 305 is established at each transmission 25 period (a period of $CLK = L$). Signals for controlling the first and second cut-off switch 212 and 213 are generated from CLK signals by three inverters 214, 215 and 218, a NOR

gate 216 and a NAND gate 217.

The first cut-off switch 212 cuts off the through-current of the CMOS inverter 305 after a predetermined period of time has passed since the rise transition time of a CLK 5 signal in each preparation period, as the cut-off switch 210 in Figure 2.

According to Figure 3, when the equalizing switch 204 is turned off in each transmission period, the CMOS inverter 305 amplifies a small voltage change in the input terminal 10 RIN. The voltage of the input terminal RIN in this case is $V_{eq} + \Delta V$ or $V_{eq} - \Delta V$, where ΔV is a small voltage magnitude. In this stage as well, since both the p-channel MOS transistor 202 and the n-channel MOS transistor 203 which constitute the CMOS inverter 305 have been turned on, a 15 through-current flows from the Vdd power line to the Vss power line through the CMOS inverter 305. This through-current is unnecessary after the voltage of the output terminal of the CMOS inverter 305 is established. Therefore, after a predetermined period of time has passed since the 20 fall transition time of a CLK signal, the second cut-off switch 213 cuts off the through-current of the CMOS inverter 305. Thus, power consumption of the receiving circuit 200b is reduced further. In addition, resistance against noise mixed from the Vdd power line and the Vss power line in each 25 transmission period can be improved.

Figure 4 shows another example of the configuration of a synchronous signal transmission circuit according to the

present invention. The signal transmission circuit in Figure 4 is a signal transmission circuit for transmitting digital signals from either one of a first circuit block group BK11, BK12, and BK13 to either one of a second circuit block group 5 BK21, BK22, and BK23 via a common signal line 30 in synchronization with a clock (CLK) signal. Each of BK11, BK12, and BK13 includes a transmitting circuit 100a with the same configuration, and each of BK21, BK22, and BK23 includes a receiving circuit 200c with the same configuration. Each 10 transmitting circuit 100a of BK11, BK12, and BK13 includes an input terminal TIN for receiving an input digital signal TD11, TD12 or TD13, a selection terminal TSEL for receiving a selection signal TS1, TS2 or TS3, and an output terminal TOUT connected to the signal line 30. Each receiving circuit 200c 15 of BK21, BK22, and BK23 includes an input terminal RIN connected to the signal line 30, a selection terminal RSEL for receiving a selection signal RS1, RS2 or RS3, and an output terminal ROUT for supplying an output digital signal RD21, RD22 or RD23. A common CLK signal is distributed to 20 all the transmitting circuits 100a and all the receiving circuits 200c.

Figure 5 shows the internal configuration of the transmitting circuit 100a in Figure 4. The transmitting circuit 100a in Figure 5 is different from the transmitting circuit 100 in Figure 1 in that the former has a logic circuit 105. The logic circuit 105 is a circuit for changing 25 each state of the input switch 102 and the transmitting

switch 103 in response to a CLK signal when a selection signal supplied to the selection terminal TSEL is activated (e.g., in the case of $TS1 = H$), and fixing each state of the input switch 102 and the transmitting switch 103 when the 5 selection signal is non-activated (e.g., in the case of $TS1 = L$). Reference numeral 106 in Figure 5 denotes an inverter for inverting an output from a NAND gate constituting the logic circuit 105. In the example shown in Figure 5, in the case of non-selection, the input switch 102 is fixed to be 10 off, and the output switch 103 is fixed to be on. However, it is also possible that in the case of non-selection, the input switch 102 is fixed to be on, and the output switch 103 is fixed to be off.

Figure 6 shows the internal configuration of the 15 receiving circuit 200c in Figure 4. The receiving circuit 200c in Figure 6 is different from the transmitting circuit 200 in Figure 1 in that the former has a logic circuit 219. The logic circuit 219 is a circuit for changing the state of the equalizing switch 204 in response to a CLK signal when a 20 selection signal supplied to the selection terminal RSEL is activated (e.g., in the case of $RS1 = H$), and fixing the state of the equalizing switch 204 to be off when the selection signal is non-activated (e.g., in the case of $RS1 = L$). Reference numeral 220 in Figure 6 denotes an inverter 25 for inverting an output from a NAND gate constituting the logic circuit 219. In the example shown in Figure 6, in the case of non-selection, the equalizing switch 204 is fixed to

be off, and two switches 205 and 208 of the latch 310 are fixed to be on and to be off, respectively.

According to the signal transmission circuits of Figures 4 to 6, a circuit block on the transmission side and 5 a circuit block on the reception side can be designated arbitrarily. For example, when a digital signal is transmitted from BK11 to BK23, TS1 = RS3 = H and TS2 = TS3 = RS1 = RS2 = L are set. At this point, the transmission of signals with a small amplitude can be achieved between the 10 transmitting circuit 100a of BK11 and the receiving circuit 200c of BK23, as in the case of Figure 1. In this case, the voltage of the signal line 30 slightly changes from V_{eq} to $V_{eq} + \Delta V$ or $V_{eq} - \Delta V$ in the signal transmission between any circuit blocks.

15 Figure 7 shows still another example of the configuration of a synchronous signal transmission circuit according to the present invention. The signal transmission circuit in Figure 7 is a signal transmission circuit for transmitting a logic operation result from the first circuit 20 block group BK31, BK32, and BK33 to the second circuit block BK41 via a common signal line 30 in synchronization with a clock (CLK) signal, which logic operation result is based on the digital signals TD31, TD32, and TD33 supplied to the first circuit block group BK31, BK32, and BK 33, respectively. 25 Each of BK31, BK32, and BK33 includes a transmitting circuit 100a in Figure 5, and BK41 includes a receiving circuit 200 in Figure 1. Each transmitting circuit 100a of BK31, BK32,

and BK33 is designed so as to receive a corresponding digital signal TD31, TD32, or TD33 at the selection terminal TSEL, and to have an input terminal TIN connected to the Vdd power line. RD41 is an output digital signal representing the 5 logic operation results.

According to the configuration of Figure 7, the logic circuit 105 (see Figure 5) in each transmitting circuit 100a changes each state of the input switch 102 and the transmitting switch 103 in response to the CLK signal when an 10 input digital signal supplied to the selection terminal TSEL is activated (e.g., in the case of TD31 = H), and fixes each state of the input switch 102 and the transmitting switch 103 when the digital signal is non-activated (e.g., in the case of TD31 = L). On the other hand, the voltage of the input 15 terminal TIN of each transmitting circuit 100a is constantly fixed to a logic high voltage (Vdd). Therefore, in the case where one of TD31, TD32, and TD33 is activated, the voltage of the signal line 30 is changed from V_{eq} to $V_{eq} + \Delta V$. In the case where two of TD31, TD32, and TD33 are activated, the voltage of the signal line 30 is changed from V_{eq} to $V_{eq} + 2 \Delta V$. In the case where three of TD31, TD32, and TD33 are activated, the voltage of the signal line 30 is changed from V_{eq} to $V_{eq} + 3 \Delta V$. These voltage changes in the signal line 20 30 appear as a change from V_{eq} to $V_{eq} - G \Delta V$, a change from V_{eq} to $V_{eq} - 2G \Delta V$, and a change from V_{eq} to $V_{eq} - 3G \Delta V$ at 25 the output terminal of the CMOS inverter 305 (see Figure 1) in the receiving circuit 200 in Figure 7. Therefore,

assuming that V_{th} is a logic threshold voltage of the inverter 206 (see Figure 1) in the latch 310, when $V_{eq} < V_{th} < V_{eq} - G\Delta V$ is satisfied, the output digital signal RD41 indicates the result of the OR operation of the three input 5 digital signals TD31, TD32 and TD33. When $V_{eq} - G\Delta V < V_{th} < V_{eq} - 2G\Delta V$ is satisfied, the output digital signal RD41 indicates the result of the majority logic operation of the three input digital signals TD31, TD32 and TD33. When $V_{eq} - 2G\Delta V < V_{th} < V_{eq} - 3G\Delta V$ is satisfied, the output digital 10 signal RD41 indicates the result of the AND operation of the three input digital signals TD31, TD32 and TD33. It is possible that the voltage of the input terminal TIN of each transmitting circuit 100a is fixed to the logic low voltage (Vss) and the logic threshold voltage of the inverter 206 in 15 the receiving circuit 200 is set to be higher than V_{eq} .

Figure 8 shows an example of the configuration of an asynchronous signal transmission circuit according to the present invention. The signal transmission circuit in Figure 8 is a signal transmission circuit for transmitting and 20 distributing digital signals (clock signals CLK in this example) from a first circuit block BK50 to each of a second circuit block group BK61, BK62, and BK63 via a common signal line 30. These circuit blocks BK50, BK61, BK62, and BK63 can be in the same semiconductor integrated circuit or in 25 different semiconductor integrated circuits.

The first circuit block BK50 includes a transmitting circuit 500 having an input terminal TIN for receiving a

clock signal to be transmitted from the internal portion of the circuit block BK50 and an output terminal TOUT connected to the signal line 30. Each of the second circuit blocks BK61, BK62, and BK63 includes a receiving circuit 600 having 5 an input terminal RIN connected to the signal line 30, an output terminal ROUT for supplying a received clock signal to the internal portion of each circuit block, and another input terminal for receiving a reset (RST) signal. A COUT terminal of each receiving circuit 600 will be described later.

Figure 9 shows the internal configuration of the transmitting circuit 500 in Figure 8. The transmitting circuit 500 in Figure 9 includes a transition detection circuit 510, a first transmitting capacitor 521, a precharge switch 522, a first transmitting switch 523, a second transmitting capacitor 531, a predischarge switch 532, a second transmitting switch 533, and two inverters 524 and 534.

The transition detection circuit 510 is a circuit for sequentially detecting a transition of the logic level of an 20 input clock (CLK) signal supplied from the input terminal TIN. This circuit includes an inverter 511, a NAND gate 512, and a NOR gate 513 so as to detect a high level period (a period of CLK = H) during which a logic high level is output to the output terminal TOUT and a low level period (a period of CLK 25 = L) during which a logic low level is output to the output terminal TOUT. The output from the NAND gate 512 is at a logic low level by a delay time of the inverter 511 from the

rise transition time of the CLK signal, i.e., a predetermined period from the start time of each high level period. The output from the NOR gate 513 is at a logic high level by a delay time of the inverter 511 from the fall transition time 5 of the CLK signal, i.e., a predetermined period from the start time of each low level period.

The first transmitting capacitor 521, the precharge switch 522, the first transmitting switch 523, and the inverter 524 constitute a high level output circuit 520. The precharge switch 522 is turned on so as to supply the logic high voltage of the Vdd power line to the first transmitting capacitor 521 for each low level period (a period of CLK = L) and is turned off for each high level period (a period of CLK = H). In other words, at each low level period, a predetermined logic high voltage is set in the first transmitting capacitor 521. The first transmitting switch 523 is turned on so as to connect the first transmitting capacitor 521 to the output terminal TOUT for a predetermined period from the start time of each high level period (a period of CLK = H). That means that at each high level period, a small positive voltage change in accordance with the voltage of the first transmitting capacitor 521 that has been set during the preceding low level period is generated in the signal line 30.

25 The second transmitting capacitor 531, the predischarge switch 532, the second transmitting switch 533, and the inverter 534 constitute a low level output circuit 530. The

5 predischarge switch 532 is turned on so as to supply the logic low voltage of the Vss power line to the second transmitting capacitor 531 for each high level period (a period of CLK = H) and is turned off for each low level period (a period of CLK = L). In other words, at each high level period, a predetermined logic low voltage is set in the second transmitting capacitor 531. The second transmitting switch 533 is turned on so as to connect the second transmitting capacitor 531 to the output terminal TOUT for a 10 predetermined period from the start time of each low level period (a period of CLK = L). That means that at each low level period, a small negative voltage change in accordance with the voltage of the second transmitting capacitor 531 that has been set during the preceding high level period is 15 generated in the signal line 30.

Figure 10 shows the internal configuration of the receiving circuit 600 in Figure 8. The receiving circuit 600 in Figure 10 includes an amplifier circuit 610, a first level circuit 620, a second level circuit 630, an equalizing control circuit 640, and a latch 650.

20 The amplifier circuit 610 includes a receiving capacitor 611, a p-channel MOS transistor 612, an n-channel MOS transistor 613, an equalizing switch 614, and an inverter 615. The p-channel MOS transistor 612 and the n-channel MOS 25 transistor 613 are inserted between the Vdd power line and Vss power line and constitute a CMOS inverter 616 for amplifying a voltage change in the input terminal RIN, i.e.,

a small voltage change in the signal line 30. The receiving capacitor 611 and the equalizing switch 614 are inserted between the input terminal and the output terminal of the CMOS inverter 616. When the equalizing switch 614 is turned 5 on, each voltage of the signal line 30 and the input terminal and the output terminal of the CMOS inverter 616 is set to a predetermined equalized voltage V_{eq} . Herein, V_{eq} is a voltage determined depending on the input/output characteristics of the CMOS inverter 616. When the 10 equalizing switch 614 is turned off, the operation of the CMOS inverter 616 for amplifying a small voltage change in the signal line 30 is allowed, so that the receiving capacitor 611 is charged and discharged.

The first level circuit 620 is a circuit for supplying 15 a first detection signal (positive logic) P when a small positive voltage change in the signal line 30 is detected. This circuit includes a p-channel MOS transistor 621 and an n-channel MOS transistor 622 that are inserted between the Vdd power line and the Vss power line. The inverter 20 constituted by these transistors 621 and 622 has a logic threshold voltage V_{th1} that is lower than the equalized voltage V_{eq} , and detects a negative voltage change in the output terminal of the CMOS inverter 616, so that a small positive voltage change in the signal line 30 is detected.

25 The second level circuit 630 is a circuit for supplying a second detection signal (negative logic) Q when a small negative voltage change in the signal line 30 is detected.

This circuit includes a p-channel MOS transistor 631 and an n-channel MOS transistor 632 that are inserted between the Vdd power line and the Vss power line. The inverter constituted by these transistors 631 and 632 has a logic 5 threshold voltage V_{thh} that is higher than the equalized voltage V_{eq} , and detects a positive voltage change in the output terminal of the CMOS inverter 616, so that a small negative voltage change in the signal line 30 is detected.

The first and second level circuits 620 and 630 can be 10 constituted based on the configuration of the CMOS inverter 616 with a modification, for example, of the gate width of the p-channel MOS transistor 612 and the n-channel MOS transistor 613 to change the current gain coefficient.

The latch 650 is a so-called RS latch, which is set and 15 reset in accordance with the first and second detection signals (P signal and Q signal) so that an output clock signal corresponding to the input clock (CLK) signal is supplied to the output terminal ROUT. This latch includes two NAND gates 651 and 652 and an inverter 653. In the 20 example shown in Figure 10, an output ROUT is set in response to the rise transition of the P signal, and the output ROUT is reset in response to the fall transition of the Q signal. To the terminal COUT, the P signal is output as it is.

The equalizing control circuit 640 is a circuit for 25 forcing the equalizing switch 614 to be on while an RST signal at a logic high level is input, the equalizing switch 614 to be on for a predetermined period after the P signal

(positive logic) or the Q signal (negative logic) is supplied, and the equalizing switch 614 to be off for other periods. This circuit includes three inverters 641, 643 and 646, and three NOR gates 642, 644 and 645. This equalizing control 5 circuit 640 is also a control circuit for resetting the output ROUT when a RST signal at a logic high level is input. The inverter 643 constitutes a delay circuit for delaying an output from the NOR gate 642.

In the signal transmission circuit shown in Figures 8
10 to 10, a RST signal in a logic high level is input to each receiving circuit 600 at the time of an initial operation. In response to this, the equalizing switch 614 is forced to be on in each receiving circuit 600. As a result, the input terminal and the output terminal of the CMOS inverter 616 are short-circuited, and each voltage of the signal line 30 and the input terminal and the output terminal of the CMOS inverter 616 is set to a predetermined equalized voltage V_{eq} . Since this voltage V_{eq} ($> V_{thl}$) is regarded as a logic high level input in the first level circuit 620, the P signal is 20 at a logic low level. On the other hand, since this voltage V_{eq} ($< V_{thh}$) is regarded as a logic low level input in the second level circuit 630, the Q signal is at the logic high level. The output voltage from the latch 650, i.e., the voltage of the output terminal ROUT, is initialized to the 25 logic low level. Then, after the RST signal is lowered to the logic low level, transmission of clock signals is started. At this point, the equalizing switch 614 is off, and the

latch 650 is holding the logic low level output.

First, the operation of each part when an input clock signal of the transmitting circuit 500 makes a transition from the logic low level to the logic high level will be described. When an input clock signal makes a rise transition, the output from the NAND gate 512 in the transition detection circuit 510 is turned to the logic low level so that the first transmitting switch 523 is on for a certain period. Therefore, a small positive voltage change in accordance with the voltage of the first transmitting capacitor 521 that has been precharged by that point of time occurs in the signal line 30. In other words, the voltage of the signal line 30 changes from V_{eq} to $V_{eq} + \Delta V$. Herein, ΔV is a voltage magnitude smaller than the signal line voltage magnitude ($V_{dd}/2$) of the conventional example described above. The CMOS inverter 616 amplifies the small positive voltage change in the signal line 30 with a gain G (= 5 to 1000). The voltage of the output terminal of the CMOS inverter 616 changes from V_{eq} toward $V_{eq} - G\Delta V$. At this point, almost all charges supplied from the first transmitting capacitor 521 to the signal line 30 rapidly transfers to the receiving capacitor 611. The first level circuit 620 detects a negative voltage change in the output terminal of the CMOS inverter 616 and changes the P signal to the logic high level. The second level circuit 630 holds the Q signal at the logic high level. Therefore, the latch 650 changes the output terminal ROUT to the logic high level. In other words, the

rise transition of an output clock signal occurs in response to the rise transition of the input clock signal. On the other hand, the equalizing control circuit 640 forces the equalizing switch 614 to be on for a certain period for 5 preparing for the fall transition of the input clock signal. As a result, the signal line 30 and the receiving circuit 600 go back to the initial states. However, the latch 650 is holding the logic high level output. On the other hand, in the transmitting circuit 500, the predischarge switch 532 10 sets the voltage of the Vss power line in the second transmitting capacitor 531.

Next, the operations of each part when an input clock signal of the transmitting circuit 500 makes a transition from the logic high level to the logic low level will be 15 described. When an input clock signal makes a fall transition, the output from the NOR gate 513 in the transition detection circuit 510 is turned to the logic high level so that the second transmitting switch 533 is on for a certain period. Therefore, a small negative voltage change 20 in accordance with the voltage of the second transmitting capacitor 531 that has been precharged by that point of time occurs in the signal line 30. In other words, the voltage of the signal line 30 changes from V_{eq} to $V_{eq} - \Delta V$. The CMOS inverter 616 amplifies the small negative voltage change in 25 the signal line 30 with a gain G . The voltage of the output terminal of the CMOS inverter 616 rapidly changes from V_{eq} toward $V_{eq} + G \Delta V$. The second level circuit 630 detects a

positive voltage change in the output terminal of the CMOS inverter 616 and changes the Q signal to the logic low level. The first level circuit 620 holds the P signal at the logic low level. Therefore, the latch 650 changes the output terminal ROUT to the logic low level. In other words, the fall transition of an output clock signal occurs in response to the fall transition of the input clock signal. On the other hand, the equalizing control circuit 640 forces the equalizing switch 614 to be on for a certain period for preparing for the rise transition of the input clock signal. As a result, the signal line 30 and the receiving circuit 600 go back to the initial states. However, the latch 650 is holding the logic low level output. On the other hand, in the transmitting circuit 500, the precharge switch 522 sets the voltage of the Vdd power line in the first transmitting capacitor 521. Thereafter, the same operation is repeated to achieve signal transmission.

As described above, according to the signal transmission circuit shown in Figures 8 to 10, an input clock signal is converted to a signal with a small amplitude on the signal line 30. Therefore, this signal transmission provides the same effect of high speed transmission, low power consumption and the like as in the case of Figure 1. A clock signal also can be distributed from any one of the circuit blocks BK61, BK62 and BK63 to another circuit block in the same manner. In order to reduce the influence of power source noise and crosstalk, it is preferable that the

asynchronous transmitting circuit 500 and receiving circuit 600 are provided in the vicinity of the peripheries of each circuit block. The asynchronous configuration shown in Figures 8 to 10 can be used for transmission of digital 5 signals other than the clock signals.

Figure 11 shows another example of the configuration of an asynchronous signal transmission circuit according to the present invention. The signal transmission circuit in Figure 11 is a signal transmission circuit for transmitting and 10 distributing a clock (CLK) signal from a first circuit block BK70 to each of a second circuit block group BK81, BK82, and BK83 via a common signal line 30. The first circuit block BK70 includes the transmitting circuit 100 shown in Figure 1. Each of the second circuit block group BK81, BK82, and BK83 15 includes the receiving circuit 600 shown in Figure 10. The input terminal TIN of the transmitting circuit 100 in BK70 is connected to the Vdd power line. Each output clock signal in BK81, BK82, and BK83 is obtained from the COUT terminal.

In the signal transmission circuit shown in Figure 11, 20 a RST signal at a logic high level is input to each receiving circuit 600 at the time of an initial operation. In response to this, the equalizing switch 614 is forced to be on in each receiving circuit 600. As a result, the input terminal and the output terminal of the CMOS inverter 616 are short-circuited, and each voltage of the signal line 30 and the 25 input terminal and the output terminal of the CMOS inverter 616 is set to a predetermined equalized voltage V_{eq} . Since

5 this voltage V_{eq} ($> V_{th1}$) is regarded as a logic high level input in the first level circuit 620, the P signal, i.e., the output voltage from the COUT terminal is turned to a logic low level. Then, after the RST signal is lowered to the logic low level, transmission of a clock signal is started. At this point, the equalizing switch 614 is off, and the COUT terminal is holding the logic low level output.

10 On the other hand, the voltage of the input terminal TIN of the transmitting circuit 100 is constantly fixed to the logic high voltage (V_{dd}). Therefore, for each transmission period (a period of $CLK = L$), the voltage of the signal line 30 changes from V_{eq} to $V_{eq} + \Delta V$. Herein, ΔV is a voltage magnitude smaller than the signal line voltage magnitude ($V_{dd}/2$) of the conventional example described above.

15 15 This voltage change in the signal line 30 appears as a change from V_{eq} to $V_{eq} - G\Delta V$ at the output terminal of the CMOS inverter 616 (see Figure 10) in the receiving circuit 600 in Figure 11. Therefore, the first level circuit 620 detects a negative voltage change in the output terminal of the CMOS

20 20 inverter 616 so as to change the P signal to the logic high level. In other words, the rise transition of the output clock signal from the COUT terminal occurs in response to the fall transition of the input clock signal. On the other hand, the equalizing control circuit 640 forces the equalizing

25 25 switch 614 to be on for a certain period for preparing for the next fall transition of the input clock signal. As a result, the signal line 30 and the receiving circuit 600 go

back to the initial states. Thus, the fall transition of the output clock signal from the COUT terminal can be obtained.

As described above, also the signal transmission circuit of Figure 11 provides the same effect of high speed transmission, low power consumption and the like as in the case of Figure 1, because an input clock signal is converted to a signal with a small amplitude on the signal line 30. The voltage of the input terminal TIN of the transmitting circuit 100 is fixed to the logic low voltage (Vss), and the Q signal of the second level circuit 630 in the receiving circuit 600 or an inverted signal thereof can be output from the COUT terminal.

The invention may be embodied in other forms without departing from the spirit or essential characteristics thereof. The embodiments disclosed in this application are to be considered in all respects as illustrative and not limiting. The scope of the invention is indicated by the appended claims rather than by the foregoing description, and all changes which come within the meaning and range of equivalency of the claims are intended to be embraced therein.

WHAT IS CLAIMED IS:

1. A signal transmission circuit for transmitting a digital signal from a first circuit block to a second circuit block via a signal line in synchronization with a clock signal that repeats a first logic level indicating a preparation period and a second logic level indicating a transmission period,

the first circuit block comprising a transmitting circuit including:

a transmitting capacitor;
an input switch for setting a voltage in accordance with a logic level of a supplied input digital signal in the transmitting capacitor at preparation period; and

a transmitting switch for generating a small voltage change in the signal line at transmission period, the voltage change being in accordance with a voltage of the transmitting capacitor that is set during a preceding preparation period,

the second circuit block comprising a receiving circuit including:

an inverter connected to the signal line;
an equalizing switch for short-circuiting the input terminal and the output terminal of the inverter so as to set a voltage of the signal line to a predetermined voltage at preparation period; and
a latch for supplying an output digital signal obtained by performing logic amplification of a voltage of the output

terminal of the inverter at transmission period.

2. A signal transmission circuit for transmitting a digital signal from a first circuit block to a second circuit block via a signal line in synchronization with a clock signal that repeats a first logic level indicating a preparation period and a second logic level indicating a transmission period,

the first circuit block comprising a transmitting circuit including:

10 a transmitting capacitor;

an input switch for setting a voltage in accordance with a logic level of a supplied input digital signal in the transmitting capacitor at preparation period; and

15 a transmitting switch for generating a small voltage change in the signal line at transmission period, the voltage change being in accordance with a voltage of the transmitting capacitor that is set during a preceding preparation period.

the second circuit block comprising a receiving circuit including:

20 an inverter connected to the signal line;

a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

25 an equalizing switch for short-circuiting the input terminal and the output terminal of the inverter so as to set a voltage of the receiving capacitor to a predetermined voltage at preparation period; and

a latch for supplying an output digital signal obtained

by performing logic amplification of a voltage of the output terminal of the inverter at transmission period.

3. A signal transmission circuit for transmitting a digital signal from a first circuit block to a second circuit block via a signal line in synchronization with a clock signal that repeats a first logic level indicating a preparation period and a second logic level indicating a transmission period,

10 the first circuit block comprising a transmitting circuit including:

a transmitting capacitor;

an input switch for setting a voltage in accordance with a logic level of a supplied input digital signal in the transmitting capacitor at preparation period; and

15 a transmitting switch for generating a small voltage change in the signal line at transmission period, the voltage change being in accordance with a voltage of the transmitting capacitor that is set during a preceding preparation period.

the second circuit block comprising a receiving circuit 20 including:

an inverter connected to the signal line;

a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

25 an equalizing switch for short-circuiting the input terminal and the output terminal of the inverter so as to set a voltage of the signal line to a predetermined voltage at preparation period; and

a latch for holding an output digital signal obtained during a preceding transmission period at preparation period.

4. A signal transmission circuit for transmitting a digital signal from a first circuit block to a second circuit block via a signal line in synchronization with a clock signal that repeats a first logic level indicating a preparation period and a second logic level indicating a transmission period,

the first circuit block comprising a transmitting circuit including:

a transmitting capacitor;

an input switch for setting a voltage in accordance with a logic level of a supplied input digital signal in the transmitting capacitor at preparation period; and

a transmitting switch for generating a small voltage change in the signal line at transmission period, the voltage change being in accordance with a voltage of the transmitting capacitor that is set during a preceding preparation period,

the second circuit block comprising a receiving circuit
20 including:

an inverter connected to the signal line;

a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

an equalizing switch for short-circuiting the input terminal and the output terminal of the inverter so as to set a voltage of the signal line to a predetermined voltage at preparation period; and

a latch for supplying an output digital signal obtained by performing logic amplification of a voltage of the output terminal of the inverter for each transmission period and holding the output digital signal obtained during a preceding transmission period for each preparation period.

5. A signal transmission circuit for transmitting a digital signal from a first circuit block to a second circuit block via a signal line in synchronization with a clock signal that repeats a first logic level indicating a preparation period and a second logic level indicating a transmission period,

the first circuit block comprising a transmitting circuit including:

a transmitting capacitor;

15 an input switch designed to be on to supply a supplied
input digital signal to the transmitting capacitor for each
preparation period so as to set a voltage in accordance with
a logic level of the input digital signal in the transmitting
capacitor at preparation period, and to be off for each
20 transmission period; and

a transmitting switch designed to be on to connect the transmitting capacitor to the signal line for each transmission period so as to generate a small voltage change in the signal line at transmission period, the voltage change being in accordance with a voltage of the transmitting capacitor that is set during a preceding preparation period, and to be off for each preparation period,

the second circuit block comprising a receiving circuit including:

an inverter connected to the signal line;

a receiving capacitor inserted between an input

5 terminal and an output terminal of the inverter;

an equalizing switch designed to be on to short-circuit the input terminal and the output terminal of the inverter for each preparation period so as to set each voltage of the signal line and the input terminal and the output terminal of the inverter to a predetermined equalized voltage at preparation period, and to be off to allow an operation of the inverter for amplifying a small voltage change in the signal line for each transmission period so as to charge and discharge the receiving capacitor; and

15 a latch for supplying an output digital signal obtained by performing logic amplification of a voltage of the output terminal of the inverter for each transmission period and holding the output digital signal obtained during a preceding transmission period for each preparation period.

20 6. The signal transmission circuit according to claim 5, further comprising a cut-off switch for separating the inverter from a power line after the setting of the equalized voltage is completed at preparation period.

7. The signal transmission circuit according to claim 25 5, further comprising a cut-off switch for separating the inverter from a power line after a voltage of the output terminal of the inverter is established at transmission

period.

8. A signal transmission circuit for transmitting a digital signal from either one of a first circuit block group to a second circuit block via a common signal line in 5 synchronization with a clock signal that repeats a first logic level indicating a preparation period and a second logic level indicating a transmission period,

each of the first circuit block group comprising a transmitting circuit including:

10 a transmitting capacitor;

an input switch designed to be on to supply a supplied input digital signal to the transmitting capacitor for each preparation period so as to set a voltage in accordance with a logic level of the input digital signal in the transmitting 15 capacitor at preparation period, and to be off for each transmission period;

a transmitting switch designed to be on to connect the transmitting capacitor to the signal line for each transmission period so as to generate a small voltage change 20 in the signal line at transmission period, the voltage change being in accordance with a voltage of the transmitting capacitor that is set during a preceding preparation period, and to be off for each preparation period; and

25 a logic circuit for changing each state of the input switch and the transmitting switch in response to the clock signal when a corresponding selection signal is activated, and for fixing each state of the input switch and the

transmitting switch when the selection signal is non-activated,

the second circuit block comprising a receiving circuit including:

5 an inverter connected to the signal line;

a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

an equalizing switch designed to be on to short-circuit the input terminal and the output terminal of the inverter
10 for each preparation period so as to set each voltage of the signal line and the input terminal and the output terminal of the inverter to a predetermined equalized voltage at preparation period, and to be off to allow an operation of the inverter for amplifying a small voltage change in the signal line for each transmission period so as to charge and
15 discharge the receiving capacitor; and

a latch for supplying an output digital signal obtained by performing logic amplification of a voltage of the output terminal of the inverter for each transmission period and
20 holding the output digital signal obtained during a preceding transmission period for each preparation period.

9. A signal transmission circuit for transmitting a digital signal from a first circuit block to either one of a second circuit block group via a common signal line in
25 synchronization with a clock signal that repeats a first logic level indicating a preparation period and a second logic level indicating a transmission period.

the first circuit block comprising a transmitting circuit including:

a transmitting capacitor;

5 an input switch designed to be on to supply a supplied input digital signal to the transmitting capacitor for each preparation period so as to set a voltage in accordance with a logic level of the input digital signal in the transmitting capacitor at preparation period, and to be off for each transmission period; and

10 a transmitting switch designed to be on to connect the transmitting capacitor to the signal line for each transmission period so as to generate a small voltage change in the signal line at transmission period, the voltage change being in accordance with a voltage of the transmitting capacitor that is set during a preceding preparation period, and to be off for each preparation period;

15 each of the second circuit block group comprising a receiving circuit including:

an inverter connected to the signal line;

20 a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

25 an equalizing switch designed to be on to short-circuit the input terminal and the output terminal of the inverter for each preparation period so as to set each voltage of the signal line and the input terminal and the output terminal of the inverter to a predetermined equalized voltage at preparation period, and to be off to allow an operation of

the inverter for amplifying a small voltage change in the signal line for each transmission period so as to charge and discharge the receiving capacitor;

5 a latch for supplying an output digital signal obtained by performing logic amplification of a voltage of the output terminal of the inverter for each transmission period and holding the output digital signal obtained during a preceding transmission period for each preparation period; and

10 a logic circuit for changing a state of the equalizing switch in response to the clock signal when a corresponding selection signal is activated, and for fixing the equalizing switch to be off when the selection signal is non-activated.

15 10. A signal transmission circuit for transmitting a logic operation result from a first circuit block group to a second circuit block via a common signal line in synchronization with a clock signal that repeats a first logic level indicating a preparation period and a second logic level indicating a transmission period, the logic operation result being based on a digital signal supplied to each of the first circuit block group,

20 each of the first circuit block group comprising a transmitting circuit including:

a transmitting capacitor;

25 an input switch designed to be on to supply a predetermined logic voltage to the transmitting capacitor for each preparation period so as to set the logic voltage in the transmitting capacitor at preparation period, and to be off

for each transmission period;

5 a transmitting switch designed to be on to connect the transmitting capacitor to the signal line for each transmission period so as to generate a small voltage change in the signal line at transmission period, the voltage change being in accordance with a voltage of the transmitting capacitor that is set during a preceding preparation period, and to be off for each preparation period; and

10 a logic circuit for changing each state of the input switch and the transmitting switch in response to the clock signal when a corresponding input digital signal is activated, and for fixing each state of the input switch and the transmitting switch when the input digital signal is non-activated,

15 the second circuit block comprising a receiving circuit including:

an inverter connected to the signal line;

a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

20 an equalizing switch designed to be on to short-circuit the input terminal and the output terminal of the inverter for each preparation period so as to set each voltage of the signal line and the input terminal and the output terminal of the inverter to a predetermined equalized voltage at 25 preparation period, and to be off to allow an operation of the inverter for amplifying a small voltage change in the signal line for each transmission period so as to charge and

discharge the receiving capacitor; and

a latch for amplifying a voltage of the output terminal of the inverter by performing logical determination with a logic threshold voltage different from the equalized voltage so that an output digital signal indicating the logic operation result is obtained for each transmission period and holding the output digital signal obtained during a preceding transmission period for each preparation period.

11. A signal transmission circuit for transmitting a digital signal from a first circuit block to a second circuit block via a signal line,

the first circuit block comprising a transmitting circuit including:

a transition detection circuit for sequentially detecting a transition of a logic level of a supplied input digital signal so as to detect a high level period during which a logic high level is output to the signal line, and a low level period during which a logic low level is output to the signal line;

20 first and second transmitting capacitors;

a precharge switch for setting a predetermined logic high voltage in the first transmitting capacitor at each low level period;

a first transmitting switch for generating a small voltage change in the signal line at each high level period, the voltage change being in accordance with a voltage of the first transmitting capacitor that is set during a preceding

low level period;

 a predischarge switch for setting a predetermined logic low voltage in the second transmitting capacitor at each high level period; and

5 a second transmitting switch for generating a small voltage change in the signal line at each low level period, the voltage change being in accordance with a voltage of the second transmitting capacitor that is set during a preceding high level period,

10 the second circuit block comprising a receiving circuit including:

 an inverter for amplifying a small voltage change in the signal line;

15 a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

 an equalizing switch inserted between the input terminal and the output terminal of the inverter;

20 a first level circuit for supplying a first detection signal when a small positive voltage change in the signal line is detected from a voltage of the output terminal of the inverter;

25 a second level circuit for supplying a second detection signal when a small negative voltage change in the signal line is detected from a voltage of the output terminal of the inverter;

 an output circuit for supplying an output digital signal having a logic level in accordance with a logic level

of the input digital signal, in accordance with the first and second detection signals; and

5 an equalizing control circuit for forcing the equalizing switch to be on for a certain period after the first detection signal or the second detection signal is supplied so as to set a voltage of the receiving capacitor to a predetermined voltage.

12. A signal transmission circuit for transmitting a digital signal from a first circuit block to a second circuit
10 block via a signal line,

the first circuit block comprising a transmitting circuit including:

15 a transition detection circuit for sequentially detecting a transition of a logic level of a supplied input digital signal so as to detect a low level period during which a logic high level is output to the signal line, and a high level period during which a logic low level is output to the signal line;

first and second transmitting capacitors;

20 a precharge switch for setting a predetermined logic high voltage in the first transmitting capacitor at each low level period;

25 a first transmitting switch for generating a small voltage change in the signal line at each high level period, the voltage change being in accordance with a voltage of the first transmitting capacitor that is set during a preceding low level period;

10 a predischarge switch for setting a predetermined logic low voltage in the second transmitting capacitor at each high level period; and

5 a second transmitting switch for generating a small voltage change in the signal line at each low level period, the voltage change being in accordance with a voltage of the second transmitting capacitor that is set during a preceding high level period,

10 the second circuit block comprising a receiving circuit including:

an inverter for amplifying a small voltage change in the signal line;

a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

15 an equalizing switch inserted between the input terminal and the output terminal of the inverter;

a first level circuit for supplying a first detection signal when a small positive voltage change in the signal line is detected from a voltage of the output terminal of the 20 inverter;

a second level circuit for supplying a second detection signal when a small negative voltage change in the signal line is detected from a voltage of the output terminal of the inverter;

25 an output circuit for supplying an output digital signal having a logic level in accordance with a logic level of the input digital signal, in accordance with the first and

second detection signals; and

an equalizing control circuit for forcing the equalizing switch to be on for a certain period after the first detection signal or the second detection signal is
5 supplied so as to set a voltage of the receiving capacitor to a predetermined voltage.

13. A signal transmission circuit for transmitting a digital signal from a first circuit block to a second circuit block via a signal line,

10 the first circuit block comprising a transmitting circuit including:

a transition detection circuit for sequentially detecting a transition of a logic level of a supplied input digital signal so as to detect a high level period during which a logic high level is output to the signal line, and a low level period during which a logic low level is output to the signal line;

first and second transmitting capacitors;

20 a precharge switch designed to be on to supply a predetermined logic high voltage to the first transmitting capacitor for each low level period so as to set the logic high voltage to the first transmitting capacitor at each low level period, and to be off for each high level period;

25 a first transmitting switch designed to be on to connect the first transmitting capacitor to the signal line for a certain period from a start time of each high level period so as to generate a small positive voltage change in

the signal line at each high level period, the voltage change being in accordance with a voltage of the first transmitting capacitor that is set during a preceding low level period;

5 a predischarge switch designed to be on to supply a predetermined logic low voltage to the second transmitting capacitor for each high level period so as to set the logic low voltage in the second transmitting capacitor at each high level period, and to be off for each low level period; and

10 a second transmitting switch designed to be on to connect the second transmitting capacitor to the signal line for a certain period from a start time of each low level period so as to generate a small negative voltage change in the signal line at each low level period, the voltage change being in accordance with a voltage of the second transmitting capacitor that is set during a preceding high level period,

15 the second circuit block comprising a receiving circuit including:

an inverter for amplifying a small voltage change in the signal line;

20 a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

an equalizing switch inserted between the input terminal and the output terminal of the inverter;

25 a first level circuit for supplying a first detection signal when a small positive voltage change in the signal line is detected from a voltage of the output terminal of the inverter;

a second level circuit for supplying a second detection signal when a small negative voltage change in the signal line is detected from a voltage of the output terminal of the inverter;

5 a latch that is set and reset in accordance with the
first and second detection signals so as to supply an output
digital signal having a logic level in accordance with a
logic level of the input digital signal; and

an equalizing control circuit for forcing the equalizing switch to be on for a certain period after the first detection signal or the second detection signal is supplied so as to set each voltage of the signal line and the input terminal and the output terminal of the inverter to a predetermined equalized voltage, and forcing the equalizing switch to be off to allow an operation of the inverter for amplifying a small voltage change in the signal line to charge and discharge the receiving capacitor for other periods.

14. The signal transmission circuit according to claim
20 13, wherein the first level circuit is constituted by an inverter having a logic threshold voltage lower than the equalized voltage, and the second level circuit is constituted by an inverter having a logic threshold voltage higher than the equalized voltage.

25 15. The signal transmission circuit according to claim
13, wherein the receiving circuit further comprises an input
terminal of a reset signal for forcing the equalizing switch

to be on.

16. A transmitting circuit for transmitting a digital signal to a signal line, comprising:

a transition detection circuit for sequentially
5 detecting a transition of a logic level of a supplied input digital signal so as to detect a high level period during which a logic high level is output to the signal line, and a low level period during which a logic low level is output to the signal line;

10 first and second transmitting capacitors;

a precharge switch designed to be on to supply a predetermined logic high voltage to the first transmitting capacitor for each low level period so as to set the logic high voltage to the first transmitting capacitor at each low level period, and to be off for each high level period;

15 a first transmitting switch designed to be on to connect the first transmitting capacitor to the signal line for a certain period from a start time of each high level period so as to generate a small positive voltage change in
20 the signal line at each high level period, the voltage change being in accordance with a voltage of the first transmitting capacitor that is set during a preceding low level period;

25 a predischarge switch designed to be on to supply a predetermined logic low voltage to the second transmitting capacitor for each high level period so as to set the logic low voltage in the second transmitting capacitor at each high level period, and to be off for each low level period; and

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a second transmitting switch designed to be on to connect the second transmitting capacitor to the signal line for a certain period from a start time of each low level period so as to generate a small negative voltage change in
5 the signal line at each low level period, the voltage change being in accordance with a voltage of the second transmitting capacitor that is set during a preceding high level period.

17. A receiving circuit for receiving a digital signal from a signal line, comprising:

10 an inverter for amplifying a small voltage change in the signal line;

a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

15 an equalizing switch inserted between the input terminal and the output terminal of the inverter;

a first level circuit for supplying a first detection signal when a small positive voltage change in the signal line is detected from a voltage of the output terminal of the inverter;

20 a second level circuit for supplying a second detection signal when a small negative voltage change in the signal line is detected from a voltage of the output terminal of the inverter;

25 a latch that is set and reset in accordance with the first and second detection signals so as to supply an output digital signal having a logic level in accordance with a logic level of the input digital signal; and

an equalizing control circuit for forcing the equalizing switch to be on for a certain period after the first detection signal or the second detection signal is supplied so as to set each voltage of the signal line and the 5 input terminal and the output terminal of the inverter to a predetermined equalized voltage, and forcing the equalizing switch to be off to allow an operation of the inverter for amplifying a small voltage change in the signal line to charge and discharge the receiving capacitor for other periods.

18. A signal transmission circuit for transmitting a clock signal from a first circuit block to each of a second circuit block group via a common signal line,

the first circuit block comprising a transmitting 15 circuit including:

a transition detection circuit for sequentially detecting a transition of a logic level of a supplied input clock signal so as to detect a high level period during which a logic high level is output to the signal line, and a low 20 level period during which a logic low level is output to the signal line;

first and second transmitting capacitors;

a precharge switch designed to be on to supply a predetermined logic high voltage to the first transmitting 25 capacitor for each low level period so as to set the logic high voltage to the first transmitting capacitor at each low level period, and to be off for each high level period;

5 a first transmitting switch designed to be on to connect the first transmitting capacitor to the signal line for a certain period from a start time of each high level period so as to generate a small positive voltage change in the signal line at each high level period, the voltage change being in accordance with a voltage of the first transmitting capacitor that is set during a preceding low level period;

10 a predischarge switch designed to be on to supply a predetermined logic low voltage to the second transmitting capacitor for each high level period so as to set the logic low voltage in the second transmitting capacitor at each high level period, and to be off for each low level period; and

15 a second transmitting switch designed to be on to connect the second transmitting capacitor to the signal line for a certain period from a start time of each low level period so as to generate a small negative voltage change in the signal line at each low level period, the voltage change being in accordance with a voltage of the second transmitting capacitor that is set during a preceding high level period,

20 each of the second circuit block group comprising a receiving circuit including:

an inverter for amplifying a small voltage change in the signal line;

25 a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

an equalizing switch inserted between the input terminal and the output terminal of the inverter;

a first level circuit for supplying a first detection signal when a small positive voltage change in the signal line is detected from a voltage of the output terminal of the inverter;

5 a second level circuit for supplying a second detection signal when a small negative voltage change in the signal line is detected from a voltage of the output terminal of the inverter:

10 a latch that is set and reset in accordance with the
first and second detection signals so as to supply an output
clock signal having a logic level in accordance with a logic
level of the input clock signal; and

an equalizing control circuit for forcing the equalizing switch to be on for a certain period after the first detection signal or the second detection signal is supplied so as to set each voltage of the signal line and the input terminal and the output terminal of the inverter to a predetermined equalized voltage, and forcing the equalizing switch to be off to allow an operation of the inverter for amplifying a small voltage change in the signal line to charge and discharge the receiving capacitor for other periods.

19. A signal transmission circuit for transmitting a
clock signal from a first circuit block to each of a second
25 circuit block group via a common signal line.

the first circuit block comprising a transmitting circuit including:

a transmitting capacitor;

an input switch designed to be on to supply a predetermined logic voltage to the transmitting capacitor for each preparation period so as to set the logic voltage in the transmitting capacitor at preparation period during which an supplied input clock signal is at a first logic level, and to be off for each transmission period during which the input clock signal is at a second logic level; and

10 a transmitting switch designed to be on to connect the transmitting capacitor to the signal line for each transmission period so as to generate a small voltage change in the signal line at transmission period, the voltage change being in accordance with a voltage of the transmitting capacitor that is set during a preceding preparation period, and to be off for each preparation period,

15 each of the second circuit block group comprising a receiving circuit including:

an inverter for amplifying a small voltage change in the signal line;

20 a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

an equalizing switch inserted between the input terminal and the output terminal of the inverter;

25 a level circuit for supplying a pulse of an output clock signal when a small voltage change in the signal line is detected from a voltage of the output terminal of the inverter; and

an equalizing control circuit for forcing the equalizing switch to be on for a certain period after the small voltage change in the signal line is detected so as to set each voltage of the signal line and the input terminal 5 and the output terminal of the inverter to a predetermined equalized voltage, and forcing the equalizing switch to be off to allow an operation of the inverter for amplifying a small voltage change in the signal line to charge and discharge the receiving capacitor for other periods.

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ABSTRACT OF THE DISCLOSURE

A signal is transmitted in synchronization with a clock signal that repeats H and L levels indicating a preparation period and a transmission period, respectively. A transmitting circuit includes a transmitting capacitor, an input switch for setting a voltage in accordance with an input digital signal in the transmitting capacitor at preparation period, and a transmitting switch for generating a small voltage change in the signal line at transmission period, the voltage change being in accordance with a voltage of the transmitting capacitor. A receiving circuit includes an inverter with a CMOS configuration, a receiving capacitor inserted between an input terminal and an output terminal of the inverter, an equalizing switch for short-circuiting the input terminal and the output terminal of the inverter so as to set the voltage of the signal line to a predetermined voltage at preparation period, and a latch for supplying an output digital signal by performing logic amplification of the voltage of the output terminal of the inverter for each transmission period, and for holding the output for each preparation period.

Fig. 1

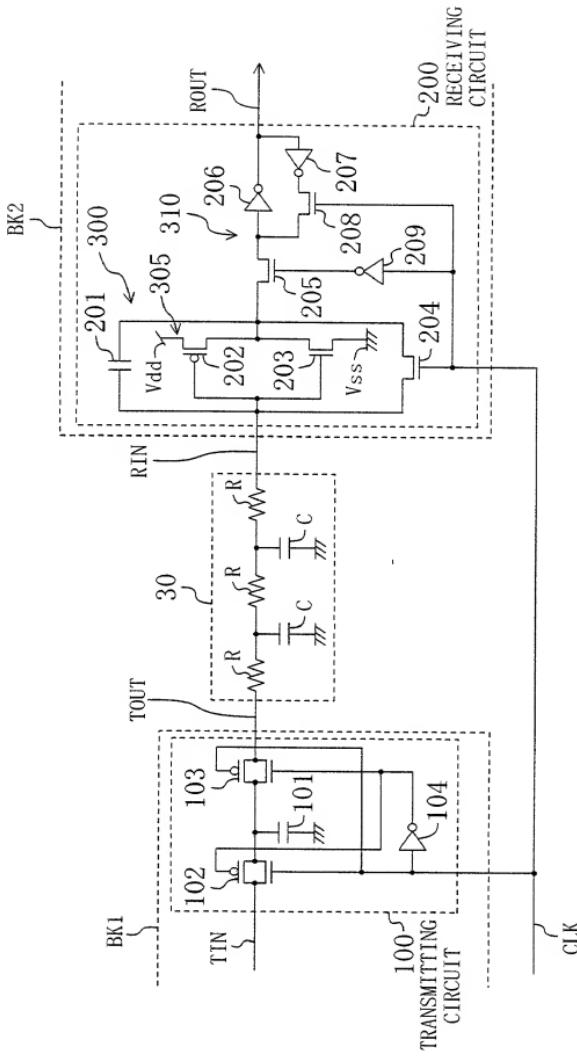


Fig. 2

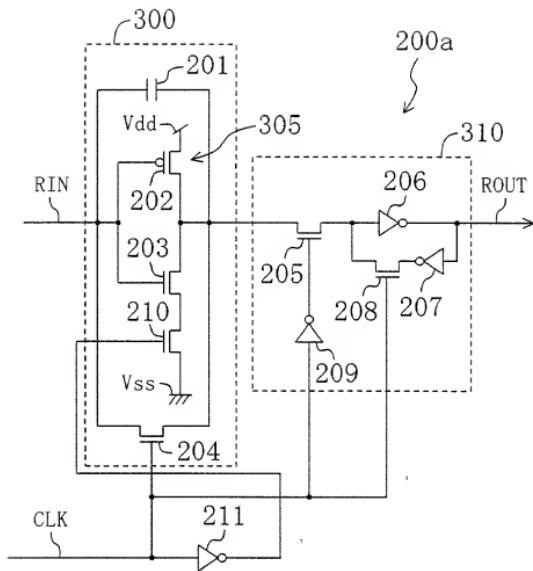
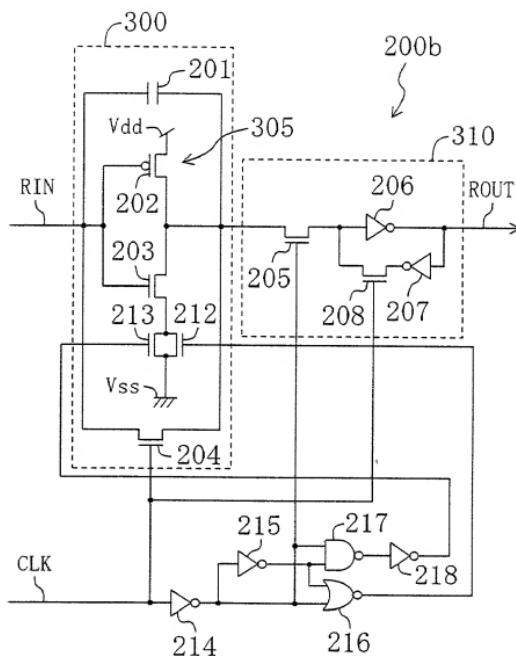


Fig. 3



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Fig. 4

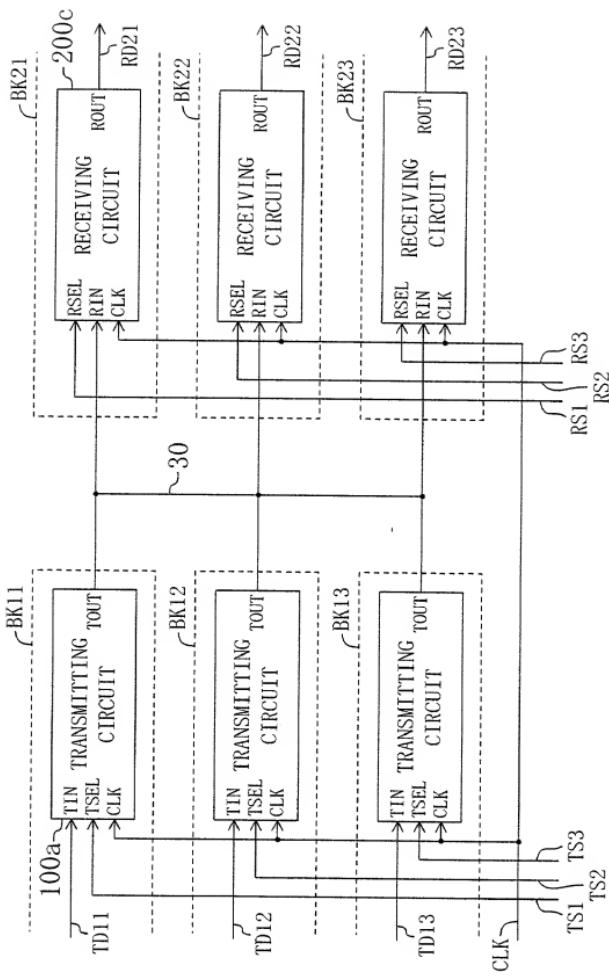


Fig. 5

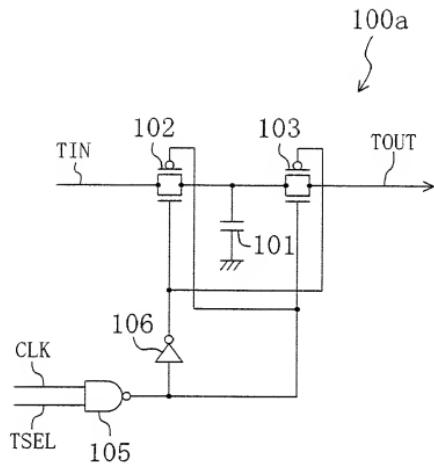


Fig. 6

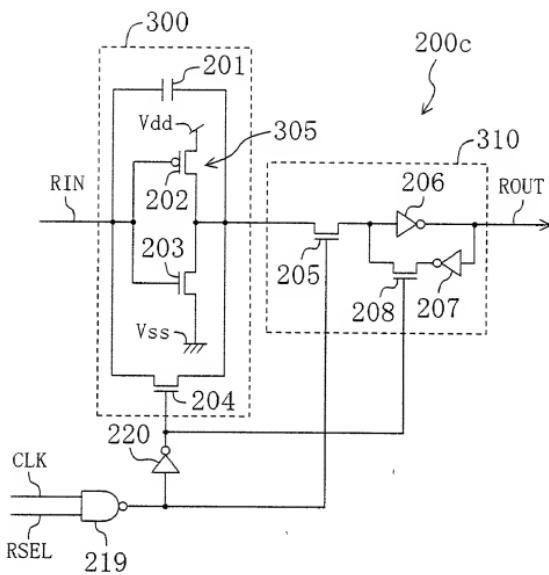


Fig. 7

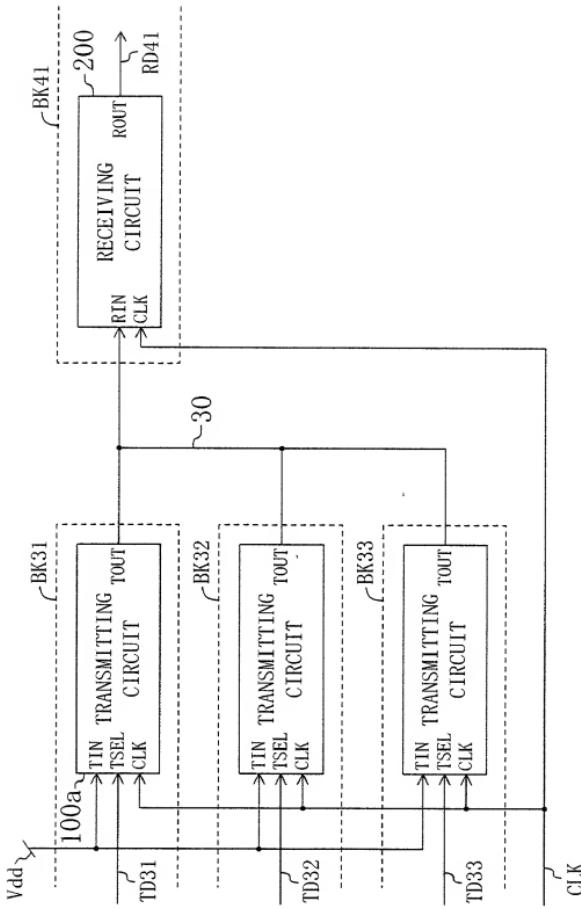


Fig. 8

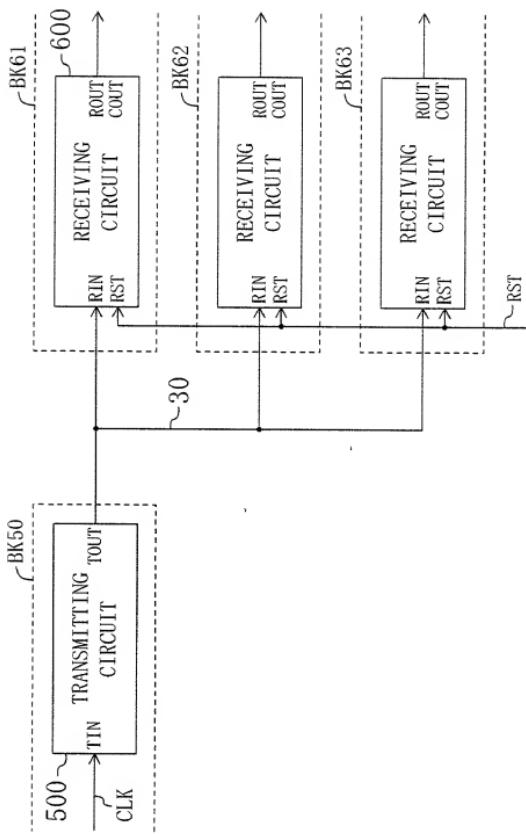
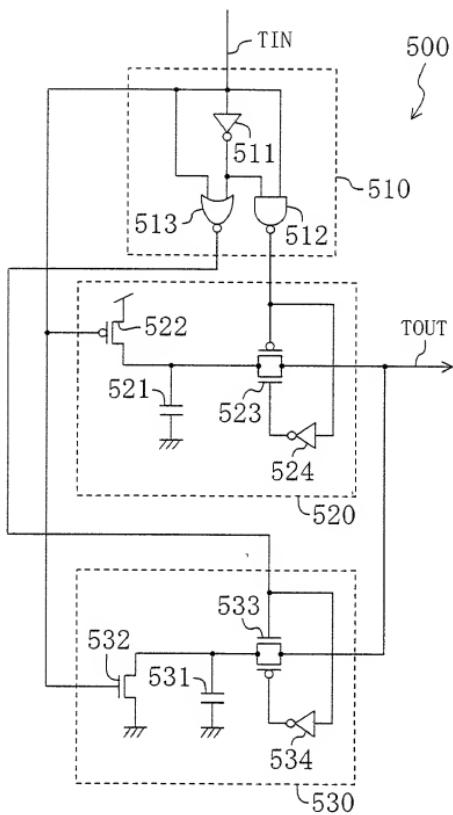


Fig. 9



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Fig. 10

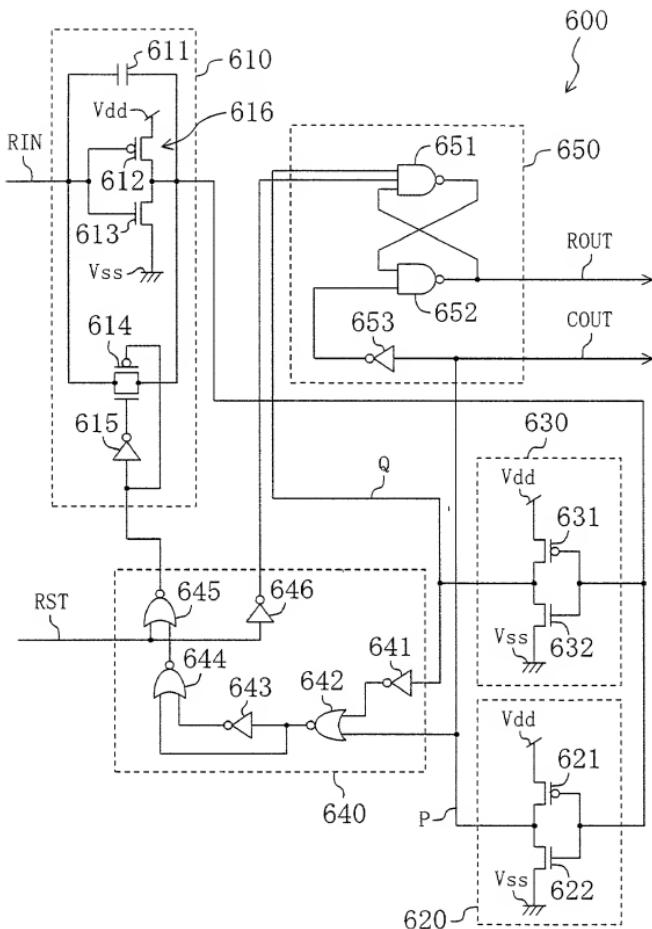
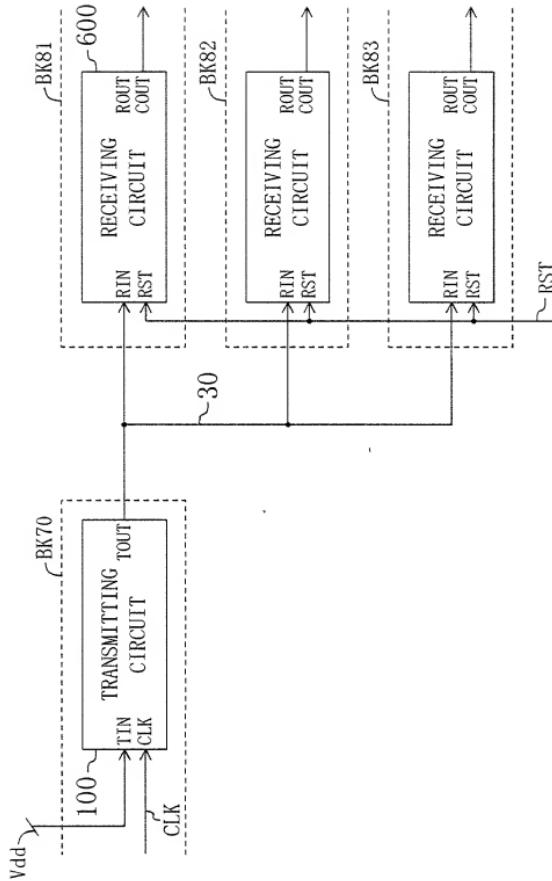


Fig. 11



Docket No. _____

**COMBINED DECLARATION/POWER OF ATTORNEY
FOR PATENT APPLICATION**

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SIGNAL TRANSMISSION CIRCUIT

_____, the specification of which

(check one) is attached hereto.

— was filed on _____ as
Application Serial No. _____.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed
11-325062 (Number)	JAPAN (Country)	16/11/1999 (Day/Month/Year Filed)	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	<input type="checkbox"/> Yes <input type="checkbox"/> No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	<input type="checkbox"/> Yes <input type="checkbox"/> No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Appln. Serial No.)	(Filing Date)	(Status-patented, pending, abandoned)
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(Appln. Serial No.)	(Filing Date)	(Status-patented, pending, abandoned)
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I hereby appoint as my attorneys, with full power of substitution and revocation, to prosecute the patent application identified above and to transact all business in the U.S. Patent and Trademark Office connected therewith: Raphael V. Lupo (Reg. No. 28,363); Jack Q. Lever, Jr. (Reg. No. 28,149); Kenneth L. Cage (Reg. No. 26,151); Stanislaus Aksman (Reg. No. 28,562); Paul Devinsky (Reg. No. 28,553); Edward E. Kubasiewicz (Reg. No. 30,020), Michael E. Fogarty (Reg. No. 36,139); Brian E. Ferguson (Reg. No. 36,801); Robert W. Zelnick (Reg. No. 36,976); and Wilhlem F. Gadiano (Reg. No. 37,136).

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The undersigned hereby authorizes the U.S. attorneys named herein to accept and follow instructions from Maeda Patent Office as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U.S. attorney and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys named herein will be so notified by the undersigned.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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* City and State, or City and Country for foreign inventors

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Keiichi KUSUMOTO et al.

Serial No.: Group Art Unit:

Filed: November 15, 2000 Examiner:

For: SIGNAL TRANSMISSION CIRCUIT

ASSOCIATE POWER OF ATTORNEY

Honorable Commissioner of
Patents and Trademarks
Washington, D. C. 20231

Sir:

The undersigned Principal Attorney of record hereby appoints the following Attorneys as his Associates with regard to the above-identified application: Stephen A. Becker, Reg. No. 26,527; John G. Bisbikis, Reg. No. 37,095; Christopher D. Bright, Reg. No. 46,578; Daniel Bucca, Reg. No. 42,368; Kenneth L. Cage, Reg. No. 26,151; Jennifer Chen, Reg. No. 42,404; Bernard P. Codd, Reg. No. 46,429; Thomas A. Corrado, Reg. No. 42,439; Lawerence T. Cullen, Reg. No. 44,489; Paul Devinsky, Reg. No. 28,553; Margaret M. Duncan, Reg. No. 30,879; Ramyar M. Farid, Reg. No. 46,692; Brian E. Ferguson, Reg. No. 36,801; Michael E. Fogarty, Reg. No. 36,139; John R. Fuisz, Reg. No. 37,327; Willem F. Gadiano, Reg. No. 37,136; Keith E. George, Reg. No. 34,111; Matthew V. Grumbling, Reg. No. 44,427; John A. Hankins, Reg. No. 32,029; Joseph Hyosuk Kim, Reg. No. 41,425; Eric J. Kraus, Reg. No. 36,190; Catherine Krupka, Reg. No. 46,227; Jack Q. Lever, Reg. No. 28,149; Raphael V. Lupo, Reg. No. 28,363; Michael A. Messina, Reg. No. 33,424; Dawn L. Palmer, Reg. No. 41,238; Joseph H. Paquin, Jr., Reg. No. 31,647; Scott D. Paul, Reg. No. 42,984; William D. Pegg, Reg. No. 42,988; Robert L. Price, Reg. No. 22,685; Thomas D. Robbins, Reg. No. 43,669; Gene Z. Robinson, Reg. No. 33,351; Joy Ann G. Serauskas, Reg. No. 27,952; Daniel H. Sherr, Reg. No. 46,425; David A. Spenard, Reg. No. 37,449; Arthur J. Steiner, Reg. No. 26,106; David L. Stewart, Reg. No. 37,578; Wesley Strickland, Reg. No. 44,363; Michael D. Switzer, Reg. No. 39,552; Leonid D. Thenor, Reg. No. 39,397; Daniel S. Trainor, Reg. No. 43,959; Cameron K. Weiffenbach, Reg. No. 44,488; Aaron

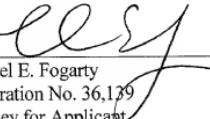
Serial No.:

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Please continue to address all communications to the undersigned.

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By 
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U.S. PATENT AND TRADEMARK OFFICE